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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,130	04/15/2004	Michel E. Bohn	BUR920040072US1	3129

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EXAMINER
LAM, NELSON C

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,130	BOHN ET AL.	
	Examiner	Art Unit	
	Nelson Lam	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ■ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Applicants' amendment to 10/709,130 has been examined. The title has been amended. Claims 1-20 are pending.

Applicants' amendment is considered persuasive in part and the applicable rejections from the prior office action along with new ground of rejection are incorporated herein.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claims 1-20 are rejected under 35 U.S.C. 102(e)** as being anticipated by Barrett et al. (US Patent Application Publication No. US 2005/0055661 A1).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As per **claim 1**, Barrett discloses a method for generating a process aid on a wafer, the method comprising the steps of:

entering a process technology and a process aid type to be built into a program ([0005]; [0006]; [0024]; [0026]; where alignment and measurement sites are process aids);

reading technology design rules and process aid parameters for the process aid type into the program ([0024]; [0025]; [0026]; [0027]);

accessing a process aid instruction file to attain instructions for building the process aid (Fig. 2, #210; [0025]; [0026]; [0027]); and

building the process aid in on the wafer using the instructions based on the technology design rules and the process aid parameters ([0028]; [0037]).

As per **claim 2**, Barrett discloses the method of claim 1, wherein the building step includes building the process aid in one of a kerf and a sacrificial die on the wafer ([0007]; [0010]).

As per **claim 3**, Barrett discloses the method of claim 1, wherein the instructions include scheme code ([0014]; [0041]; [0042], where Java software is a form of scheme code).

As per **claim 4**, Barrett discloses the method of claim 1, further comprising the step of documenting the process aid ([0022]; Fig. 1, #120; Fig. 2, #130; [0027]).

As per **claim 5**, Barrett discloses the method of claim 4, wherein the documentation includes process aid location ([0020]; [0024]).

As per **claim 6**, Barrett discloses the method of claim 1, further comprising at least one of the steps of verifying the process aid against production data and testing the process aid ([0033]; Fig. 2, #265; [0034]).

As per **claim 7**, Barrett discloses the method of claim 1, further comprising the step of rerunning the step of building ([0040]).

As per **claim 8**, Barrett discloses a system for generating a process aid on a wafer (Fig. 1; [0022]), the system comprising:

means for entering a process technology and a process aid type into a program ([0005]; [0006]; [0024]; [0026]; where alignment and measurement sites are process aids);

means for reading technology design rules and process aid parameters for the process aid into the program ([0024]; [0025]; [0026]; [0027]);

means for accessing a process aid instruction file to attain instructions for building the process aid (Fig. 2, #210; [0025]; [0026]; [0027]); and

means for building the process aid on the wafer using the instructions based on the technology design rules and process aid parameters ([0028]; [0037]).

As per **claim 9**, Barrett discloses the system of claim 8, wherein the process aid is one of an electrical device and an optical device ([0005]; [0006]).

As per **claim 10**, Barrett discloses the system of claim 8, wherein the instructions include scheme code ([0014]; [0041]; [0042], where Java software is a form of scheme code).

As per **claim 11**, Barrett discloses the system of claim 8, further comprising means for documenting the process aid ([0022]; Fig. 1, #120; Fig. 2, #130; [0027]).

As per **claim 12**, Barrett discloses the system of claim 11, wherein the documentation includes process aid location ([0020]; [0024]).

As per **claim 13**, Barrett discloses the system of claim 8, further comprising means for verifying the process aid against production data ([0033]; Fig. 2, #265; [0034]).

As per **claim 14**, Barrett discloses the system of claim 8, further comprising means for testing the process aid ([0033]; Fig. 2, #265; [0034]).

As per **claim 15**, Barrett discloses a computer useable medium program product comprising a computer having computer readable program code embodied therein for generating a process aid on a wafer ([0014]; [0023]), the program product comprising:

program code configured to allow entering a process technology and the process aid type ([0005]; [0006]; [0024]; [0026]; where alignment and measurement sites are process aids);

program code configured to read technology design rules and process aid parameters for the process aid ([0024]; [0025]; [0026]; [0027]);

program code configured to access a process aid instruction file to attain instructions for building the process aid (Fig. 2, #210; [0025]; [0026]; [0027]); and

program code configured to build the process aid on the wafer using the instructions based on the technology design rules and process aid parameters ([0028]; [0037]).

As per **claim 16**, Barrett discloses the program product of claim 15, wherein the process aid is one of an electrical device and an optical device ([0005]; [0006]).

As per **claim 17**, Barrett discloses the program product of claim 15, wherein the instructions include scheme code ([0014]; [0041]; [0042], where Java software is a form of scheme code).

As per **claim 18**, Barrett discloses the program product of claim 15, further comprising program code configured to document the process aid ([0022]; Fig. 1, #120; Fig. 2, #130; [0027]).

As per **claim 19**, Barrett discloses the program product of claim 15, further comprising program code configured to verify the process aid against production data ([0033]; Fig. 2, #265; [0034]).

As per **claim 20**, Barrett discloses the program product of claim 15, further comprising program code configured to test the process aid ([0033]; Fig. 2, #265; [0034]).

Remarks

4. Applicants states Barrett does not disclose entering a process technology and a process aid type to be build into a program, reading technology design rules and process aid parameters for the process aid type into the program, accessing a process aid instruction file to attain instructions for building the process aid, and building the process aid in on the wafer using the instructions based on the technology design rules and the process aid parameters.

Respectfully, the Examiner does not agree and the Applicants are directed to the following cites:

Paragraphs [0005], [0006], [0024] and [0026] of Barrett discloses entering process technologies and alignment and measurements sites and processing assist features which are process aids.

Paragraphs [0024], [0025], [0026] and [0027] of Barrett describes a Graphical User Interface (GUI) that stores and a database that retrieves or reads processing parameters which suggests reading technology design rules and processing assist features which are process aid type into the program.

Fig. 2, #210 in combination with paragraphs [0025], [0026] and [0027] of Barrett discloses software design manipulation utilities to perform functions on processing assist features which suggests instructions for building the process aid.

Paragraphs [0028] along with [0037] of Barrett teaches a kerf creation process concurrently with the chip design manipulation process or process aids and mask build process. This would suggest building the process aid in on the wafer using the instructions based on the technology design rules and the process aid parameters.

Therefore, based on the identified and referenced explanatory cites in the non-final and instant office action, the rejection under 35 USC 102(e) is maintained.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nelson Lam whose telephone number is 571 272-8318. The examiner can normally be reached on Monday-Friday from 9am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nelson Lam

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Assistant Examiner
Art Unit 2825

Jack K. Chiang

JACK CHIANG
SUPERVISORY PATENT EXAMINER